UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,276	01/17/2002	Timothy A. Pontius	US028004	4828

7590 08/13/2004

Corporate Patent Counsel
U.S. Philips Corporation
580 White Plains Road
Tarrytown, NY 10591

EXAMINER	
LEFKOWITZ, SUMATI	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,276	PONTIUS ET AL.	
	Examiner	Art Unit	
	Sumati Lefkowitz	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The use of the word asynchronous is inconsistent with its accepted meaning (see 112/2nd paragraph rejection below) and so should be amended to more accurately reflect the claimed invention.

3. The abstract of the disclosure is objected to because the use of the word asynchronous is inconsistent with its accepted meaning (see 112/2nd paragraph rejection below) and so should be amended to more accurately reflect the claimed invention.

Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because the use of the word asynchronous is inconsistent with its accepted meaning (see 112/2nd paragraph rejection below) and so should be amended to more accurately reflect the claimed invention.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "asynchronous" in the claims is used by the claim to mean "delayed with respect to a clock", while the accepted meaning is "not related to the clock in any way." The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 4, 5, 7-10, 12, 13, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeddeloh et al., 5,692,165 (hereinafter Jeddeloh).

a. As to claims 1 and 8, Jeddeloh discloses a system comprising: a plurality of functional blocks (note Figures 3 and 4, processor 20, system controller 50, memory control 60 and memory 40 and abstract, memory controller and memory devices), and a bus structure (note Figure 3, element 25 and Figure 4, memory control lines from memory control 60 to memory 40)

that is configured to facilitate communications among the plurality of functional blocks, wherein at least one functional block (i.e., system controller 50) of the plurality of functional blocks includes a bus interface adapter (i.e., host bus control 52, arbitration control 56 and memory control 60) that is configured to provide either of two modes of operation, such that communications via the bus structure are synchronous in a first mode of operation, and asynchronous in a second mode of operation (note abstract, Figures 5, 6, 7 and column 9, lines 26-56, column 10, line 26 - column 11, line 26, wherein the programmable delay input without a delay element, i.e., input 0 of the MUX in Figure 7 reads on a synchronous mode of operation and any other inputs including delay elements, i.e., inputs 1 to N-1 of the MUX in Figure 7 read on the claimed asynchronous mode of operation).

b. As to claims 2 and 9, Jeddeloh discloses that the bus interface adapter includes at least one delay device (note Figure 7 and column 11, lines 1-26) for delaying control signals (note abstract and column 9, lines 26-37) that are communicated via the bus, and the at least one delay device is configured to be bypassed (note Figure 7, input 0 of MUX, without delay element) during the first mode of operation, and used for delaying control signals (note Figure 7, inputs 1 to N-1 of the MUX) during the second mode of operation.

c. As to claim 4, Jeddeloh discloses that the system further includes a bus controller (note Figure 3, element 50 and Figure 4) that is configured to control the communications among the plurality of functional blocks, and includes a plurality of bus interface modules (i.e., inherent that any device coupled to a bus would include bus interface circuitry for communicating over the bus), at least one bus interface module of the plurality of bus interface modules being configured to selectively provide either synchronous communications or asynchronous

communications via the bus structure (note abstract, Figures 5, 6, 7 and column 9, lines 26-56, column 10, line 26 - column 11, line 26, wherein the programmable delay input without a delay element, i.e., input 0 of the MUX in Figure 7 reads on a synchronous mode of operation and any other inputs including delay elements, i.e., inputs 1 to N-1 of the MUX in Figure 7 read on the claimed asynchronous mode of operation).

d. As to claims 5 and 10, Jeddeloh discloses that the bus controller includes one or more delay devices (note Figure 7 and column 9, lines 26-37 and column 11, lines 1-26) that are configured to delay control signals that are communicated among the plurality of functional blocks, thereby facilitating communication of data between a first functional block and a second functional block of the plurality of functional blocks using an asynchronous communication with the first functional block and a synchronous communication with the second functional block (note column 10, lines 12-67 and column 15, line 36 – column 16, line 6, wherein if no delay is required, it reads on synchronous communication and if a delay is required, it reads on asynchronous communication).

e. As to claims 7 and 12, Jeddeloh discloses that the bus controller is further configured to: determine if communications with the at least one functional block can be effected via synchronous communications, and cause the bus interface adapter to enter the second mode of operation only if communications with the at least one functional block cannot be effected via synchronous communications (note abstract and column 14, line 31 – column 17, line 37, wherein the determination of appropriate delay values reads on determining if communications can be effected via synchronous communications (i.e., no delay is required) or if it cannot be effected via synchronous communications (i.e., a delay is required).

f. As to claim 13, the claim limitations have already been discussed with respect to claims 1 and 8, with the exception of creating a layout of functional blocks and the determination of the clock skew associated with at least one functional block based on the layout.

With respect to creating a layout of functional blocks, Jeddeloh inherently creates a layout of a plurality of functional blocks by choosing to design his system as he does, i.e., in selecting a system, Jeddeloh inherently creates a layout of functional blocks.

As for the determination of the clock skew associated with at least one functional block, the selective configuration by Jeddeloh of the functional block for operation in one mode or another, i.e., synchronous (without delay) or asynchronous mode (with delay), implies that a clock skew associated with a functional block is determined, since the clock skew would have to be determined in order to determine what kind of delay, if any, to impose on the control signals (note column 4, line 47 – column 6, line 4).

g. As to claims 15 and 16, the claim limitations have already been discussed with respect to claims 4 and 5 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 3, 6, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh et al., 5,692,165 (hereinafter Jeddeloh) in view of Gheewala et al., 6617621 (hereinafter Gheewala).

As to claims 3, 6, 11, and 14, Jeddeloh discloses that {3}: the at least one functional block is embodied in an integrated circuit and that {6,11,14}: the bus controller is embodied in an integrated circuit (note column 6, lines 30-35 and column 7, lines 36-47) but fails to disclose that {3}: the at least one functional block is embodied in an integrated circuit that includes a plurality of conductive layers, and the bus interface adapter is configured to provide either the first or the second mode of operation based on a configuration of interconnections at an upper layer of the plurality of conductive layers or that {6,11,14}: the bus controller is embodied in an integrated circuit that includes a plurality of conductive layers, and the at least one bus interface module is configured to selectively provide either the synchronous or the asynchronous communications based on a configuration of interconnections at an upper layer of the plurality of conductive layers.

Gheewala discloses that integrated circuits are comprised of a plurality of conductive layers and that the upper layers are where customization based on a user's preferences is performed (note column 2, line 60 – column 3, line 48).

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the integrated circuits of Jeddeloh to comprise a plurality of conductive layers, the upper layers of which comprise user customizable layers, as Gheewala teaches, thereby allowing the selective provision of either synchronous or asynchronous communications in Jeddeloh, so as to allow for faster turn around time, fewer masks, and reduced mask costs for fabrication, as Gheewala teaches in the abstract and column 3, lines 18-22.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the prior art teaches or suggests clock skew compensation/adjustment.

US PG-PUBS: 2003/0046598 A1 Crafts et al.

US Patents:

6,484,268	Tamura et al.	5,987,619	Hamamoto et al.
5,935,257	Nishimura	5,857,095	Jeddeloh et al.
5,819,076	Jeddeloh et al.	5,745,533	Asada et al.
5,615,358	Vogley	5,608,896	Vogley
5,293,626	Priest et al.	5,272,729	Bechade et al.
4,839,907	Saneski		

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-872-9306 for Official communications

703-746-5661 for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Sumati Lefkowitz
Primary Examiner
Art Unit 2112

sl
August 9, 2004